Zynq를 활용한 SoC / FPGA 설계

HDL 및 HLS를 이용한 설계 이해 및 실습

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CONTENTS

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SoC 설계 이론

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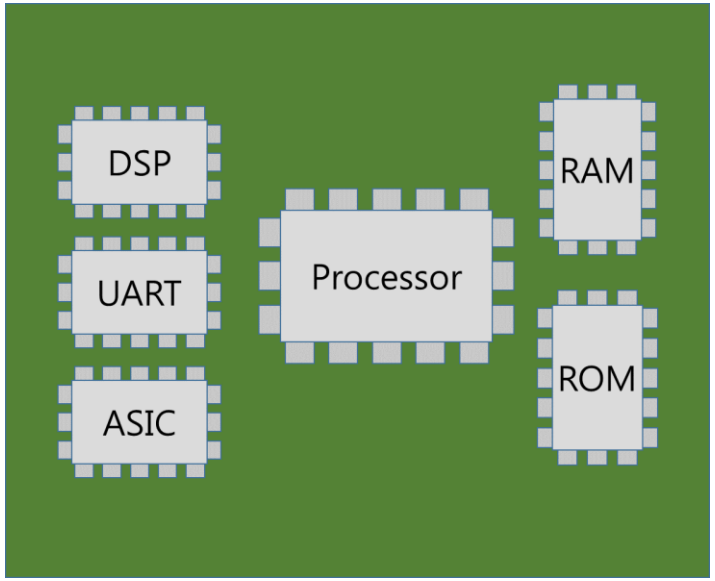
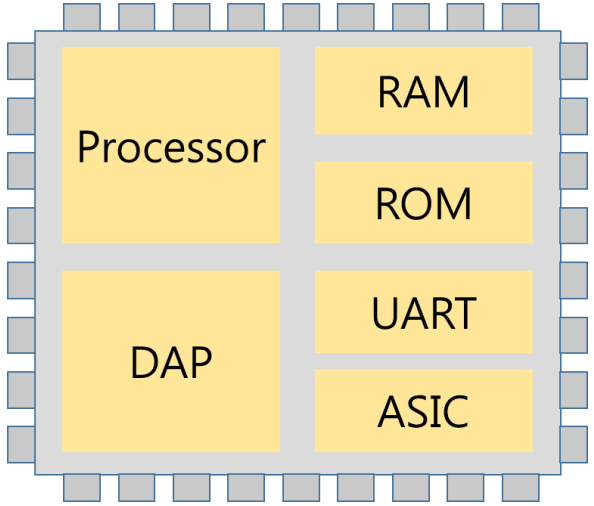
01. SoC(System on Chip)

- 시스템을 단일 칩에 구현한 집적회로(IC)





시스템(PCB 수준)

Programmable Processor,
메모리, 버스, SW

단일 칩

크기↓ 전력↓ 신뢰성↑

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Challenges in SoC

- Time-to-market ↓
  - 빠른 시장 진입 시간
  - 개발, 검증 소요기간 단축 필요

→주어진 시간이 짧음

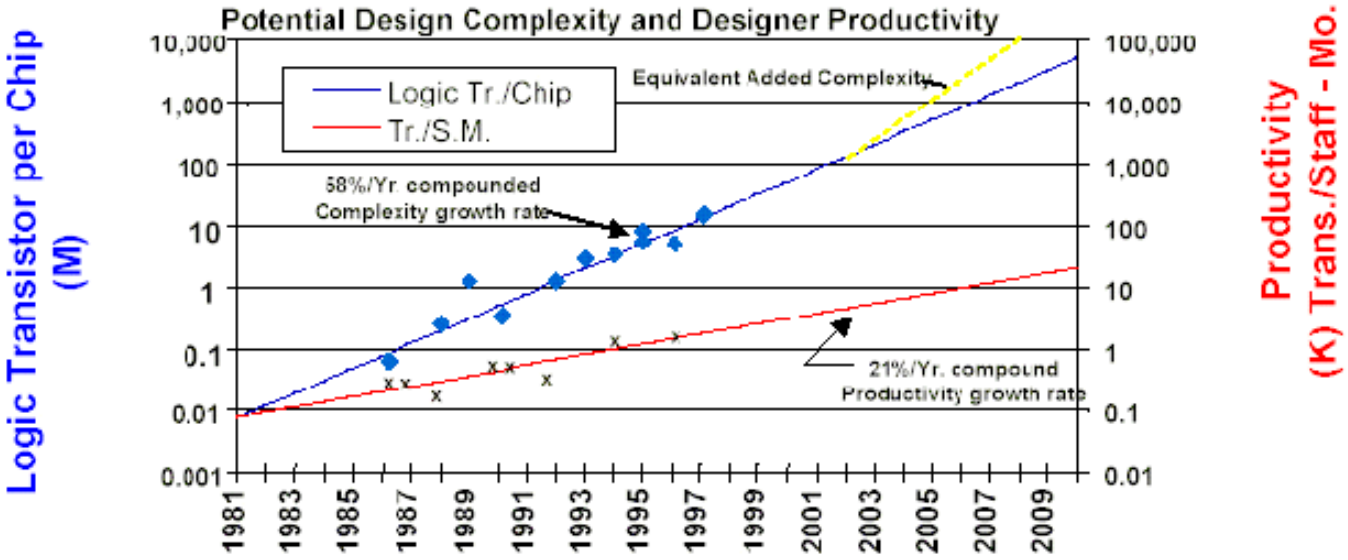
- 시스템 복잡성 ↑
  - 높은 집적도, 많은 컴포넌트

→소요되는 시간은 매우 큼

설계 속도 << 시장 요구

생산성 격차
(productivity gap) 증가

Gap is increasing



Year	Technology	Chip Complexity	Frequency	3 Yr. Design Staff	Staff Cost*
1997	250 nm	13 M Tr.	400	210	90 M
1998	250 nm	20 M Tr.	500	270	120 M
1999	180 nm	32 M Tr.	600	360	160 M
2002	130 nm	130 M Tr.	800	800	360 M

* @ $150K / Staff Yr. (In 1997 Dollars)

생산성 증가율 < 시스템 복잡성 증가율

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02. IP, 재사용 기반 설계

- IP(Intellectual Property, 설계 자산)
- 기능 블록 단위로 HW IP와 SW IP로 나뉨
- HW IP
  - Soft IP: Verilog, VHDL 등의 HW 기술언어로 구현
  - Firm IP: 합성된 게이트 수준의 Netlist
  - Hard IP: 공정 규칙에 따라 Layout이 완성된 IP

IP 형식	설계 자료 형태	최적화 정도	공정 의존도	Reusability
Hard	GDSII	매우 높음	공정에 절대 의존	낮음
Firm	Targeted netlist	높음	공정 의존	높음
Soft	RTL	낮음	공정 의존도 없음	매우 높음

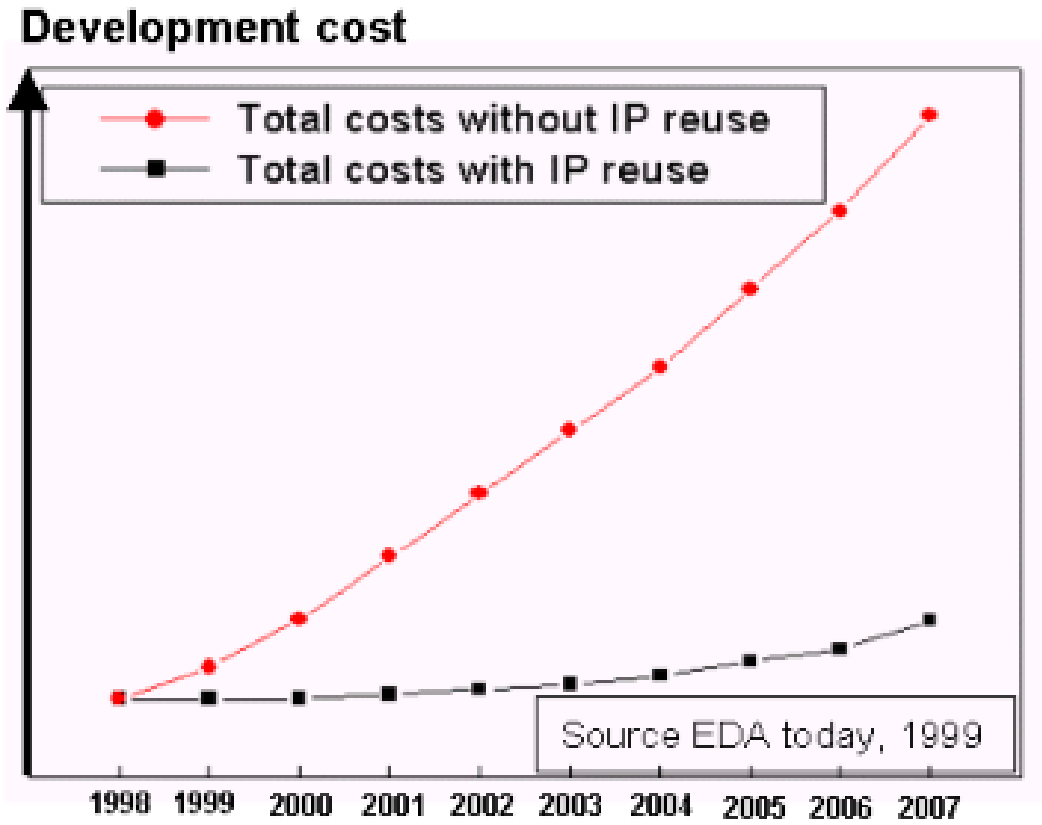
HW IP 종류

IP ReUse

- IP 재사용
  - 설계 시 검증된 IP를 사용
  - 수정, 재검증 최소화

→시간, 비용 절감

- 시스템 복잡도 증가
  - IP 재사용 않을 경우 비용 매우 크게 증가



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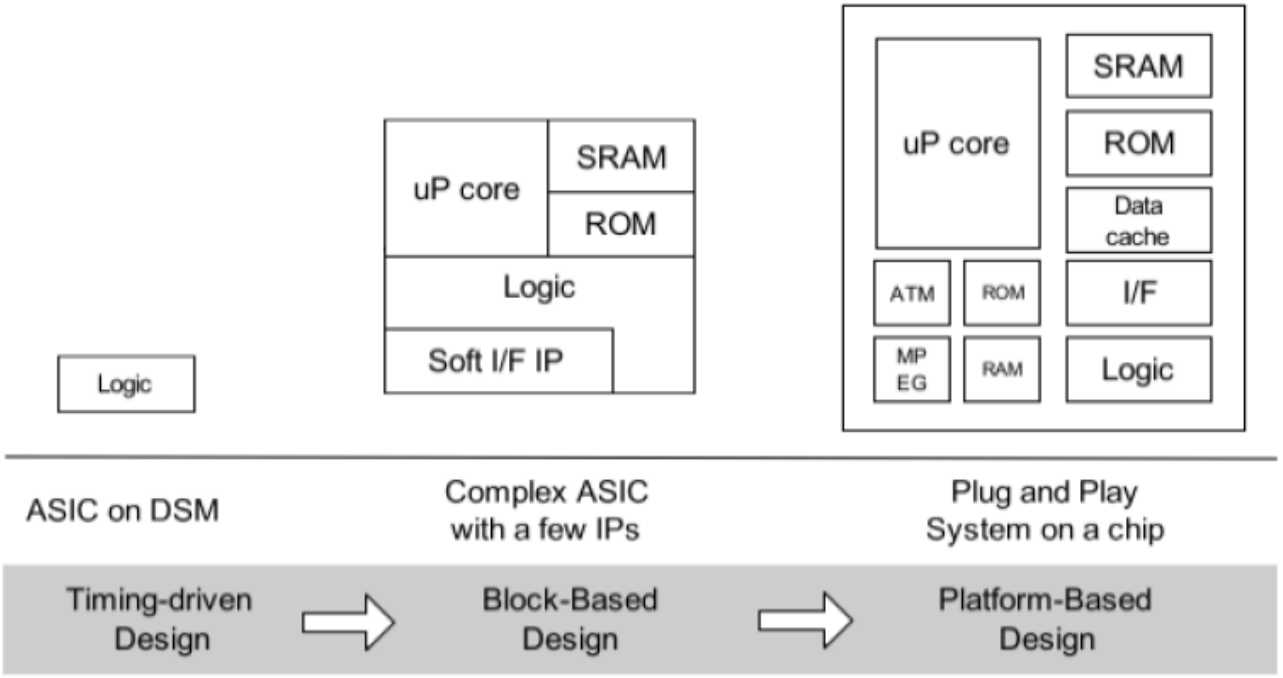
Design Reuse

- BBD(Block-Based-Design)
  - 검증된 IP로 시스템 구성
  - IP 재사용

- IP 재사용의 한계

→구성, 재검증 비용

- PBD(Platform-Based-Design)
  - 범용적 플랫폼 구성
  - 플랫폼 재사용



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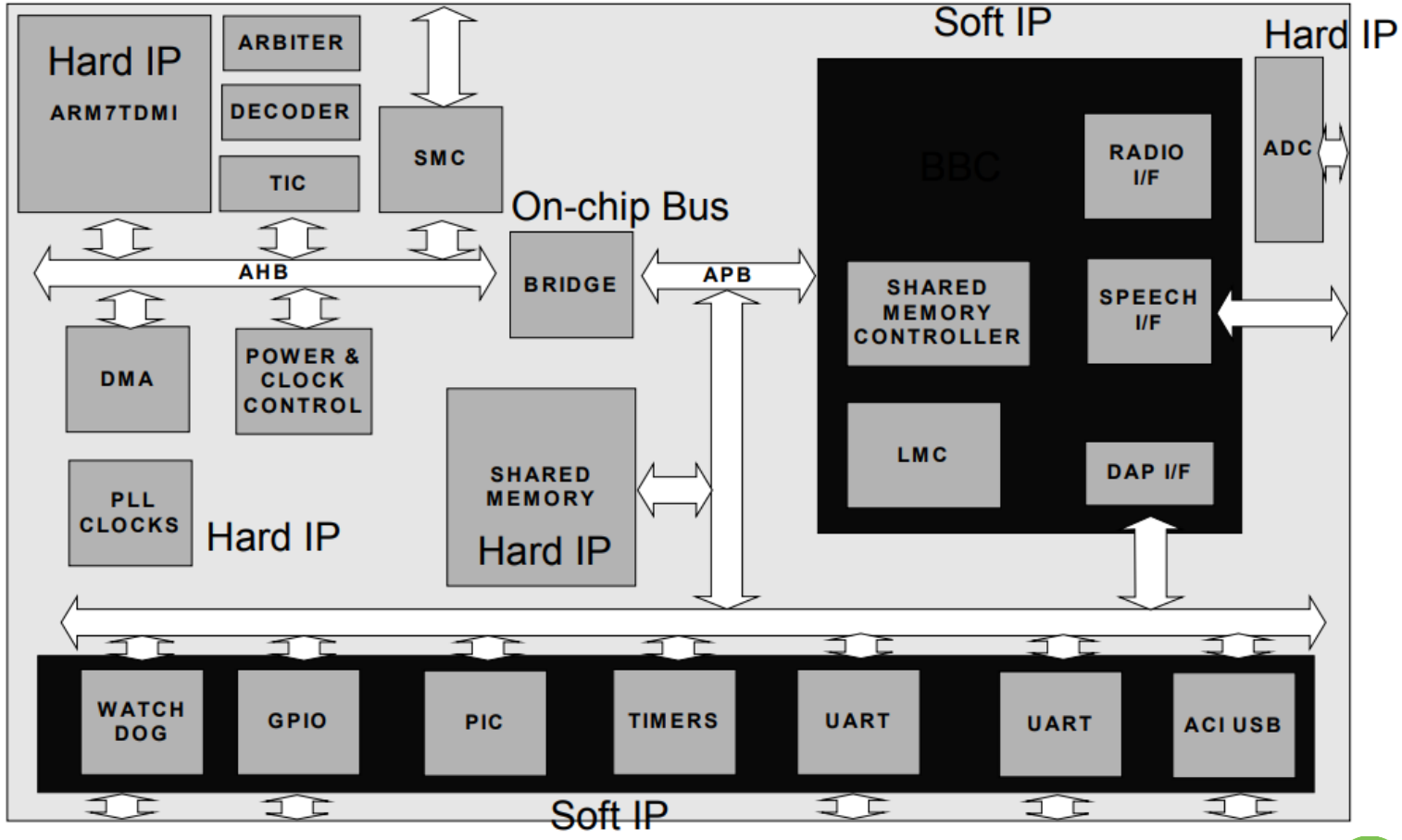
Platform Based Design

- 같은 분야(application space)일 경우 하나의 플랫폼을 여러 제품에 응용 가능

- ex) 블루투스 플랫폼
  - 이어폰/스피커
  - 마우스/키보드



source: University of British Columbia

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Processor + FPGA

- 프로세서 + FPGA
  - 외부 인터페이스를 사용해 프로세서와 FPGA 간 연결
  - HW IP를 FPGA에 구현하여 높은 성능, IP 추가 변경 용이
- 단점
  - Host, FPGA 보드를 각각 사용하는 경우 많은 비용
  - 인터페이스, 부품 선정에 대한 시간적 소모

- External bus interface
- PCIe
- AMBA

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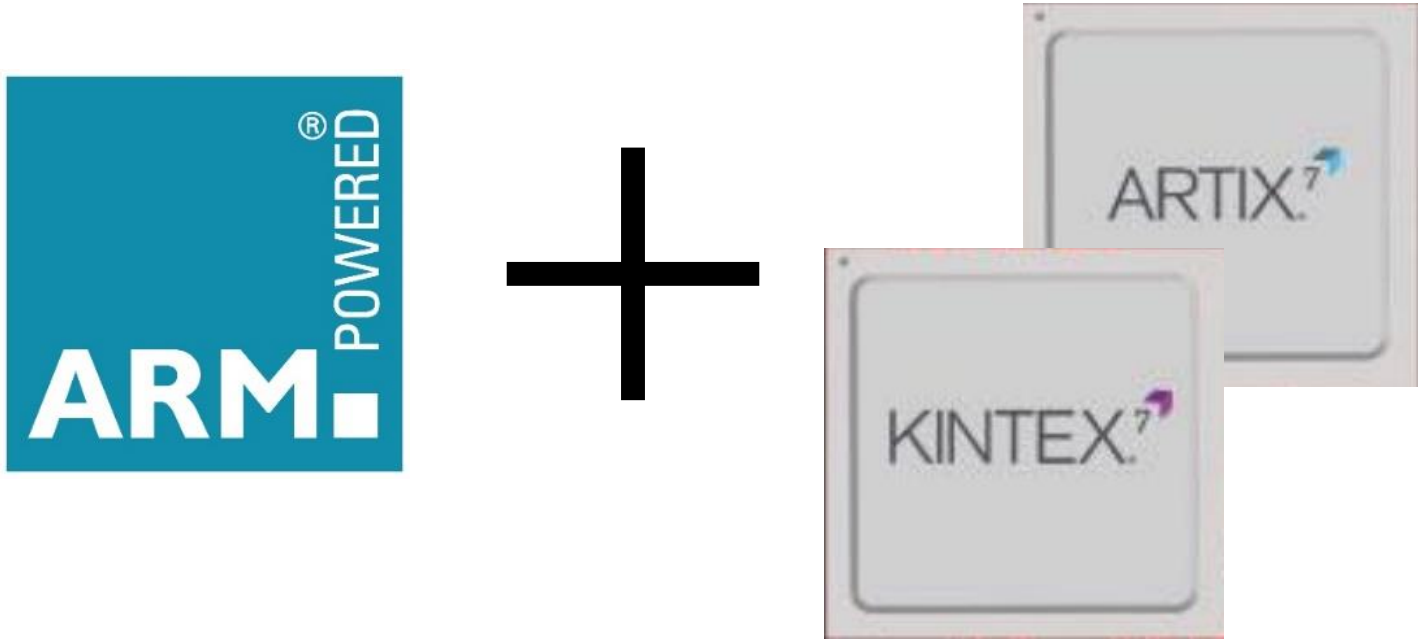
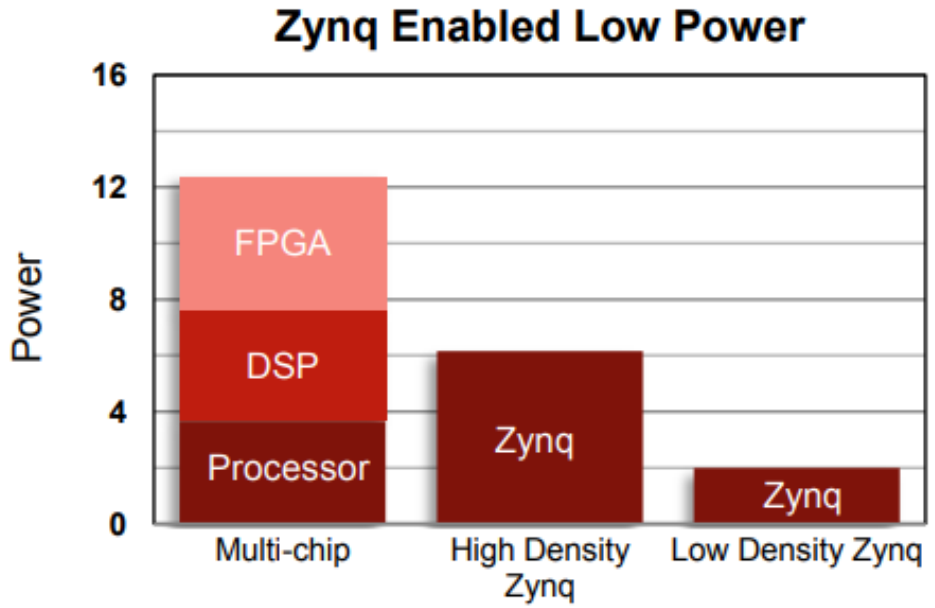
Zynq Platform



- Software & Hardware Programmable
  - 개발 시간 단축
  - Flexibility(제품의 유연성)
  - 가격, 성능 이점

Platform Comparison



	ASIC	ASSP	2 Chip Solution	Zynq-7000
Performance	+	+	■	+
Power	+	+	-	+
Unit Cost	+	+	-	■
TCO	■	+	+	+
Risk	-	+	+	+
TTM	-	+	+	+
Flexibility	-	-	+	+
Scalability	-	■	+	+

- Zynq
  - 성능, 전력 소모량 이점
  - 개발 시 리스크 감소, 수정 가능해 유연성 높음

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Zynq-7000 SoC Family

		Cost-Optimized Devices						Mid-Range Devices			
	Device Name	Z-7007S	Z-7012S	Z-7014S	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
	Part Number	XC7Z007S	XC7Z012S	XC7Z014S	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z035	XC7Z045	XC7Z100
Processing System (PS)	Processor Core	Single-Core ARM® Cortex™-A9 MPCore™ Up to 766MHz			Dual-Core ARM Cortex-A9 MPCore Up to 866MHz			Dual-Core ARM Cortex-A9 MPCore Up to 1GHz[1]			
	Processor Extensions	NEON™ SIMD Engine and Single/Double Precision Floating Point Unit per processor									
	L1 Cache	32KB Instruction, 32KB Data per processor									
	L2 Cache	512KB									
	On-Chip Memory	256KB									
	External Memory Support[2]	DDR3, DDR3L, DDR2, LPDDR2									
	External Static Memory Support[2]	2x Quad-SPI, NAND, NOR									
	DMA Channels	8 (4 dedicated to PL)									
	Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO									
	Peripherals w/ built-in DMA[2]	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO									
	Security[3]	RSA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot									
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts									
Programmable Logic (PL)	7 Series PL Equivalent	Artix®-7	Artix-7	Artix-7	Artix-7	Artix-7	Artix-7	Kintex®-7	Kintex-7	Kintex-7	Kintex-7
	Logic Cells	23K	55K	65K	28K	74K	85K	125K	275K	350K	444K
	Look-Up Tables (LUTs)	14,400	34,400	40,600	17,600	46,200	53,200	78,600	171,900	218,600	277,400
	Flip-Flops	28,800	68,800	81,200	35,200	92,400	106,400	157,200	343,800	437,200	554,800
	Total Block RAM (# 36Kb Blocks)	1.8Mb (50)	2.5Mb (72)	3.8Mb (107)	2.1Mb (60)	3.3Mb (95)	4.9Mb (140)	9.3Mb (265)	17.6Mb (500)	19.2Mb (545)	26.5Mb (755)
	DSP Slices	66	120	170	80	160	220	400	900	900	2,020
	PCI Express®	—	Gen2 x4	—	—	Gen2 x4	—	Gen2 x4	Gen2 x8	Gen2 x8	Gen2 x8
	Analog Mixed Signal (AMS) / XADC[2]	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs									
	Security[3]	AES & SHA 256b Decryption & Authentication for Secure Programmable Logic Config									
	Speed Grades: Commercial	-1			-1			-1			-1
	Speed Grades: Extended	-2			-2,-3			-2,-3			-2
	Speed Grades: Industrial	-1, -2			-1, -2, -1L			-1, -2, -2L			-1, -2, -2L

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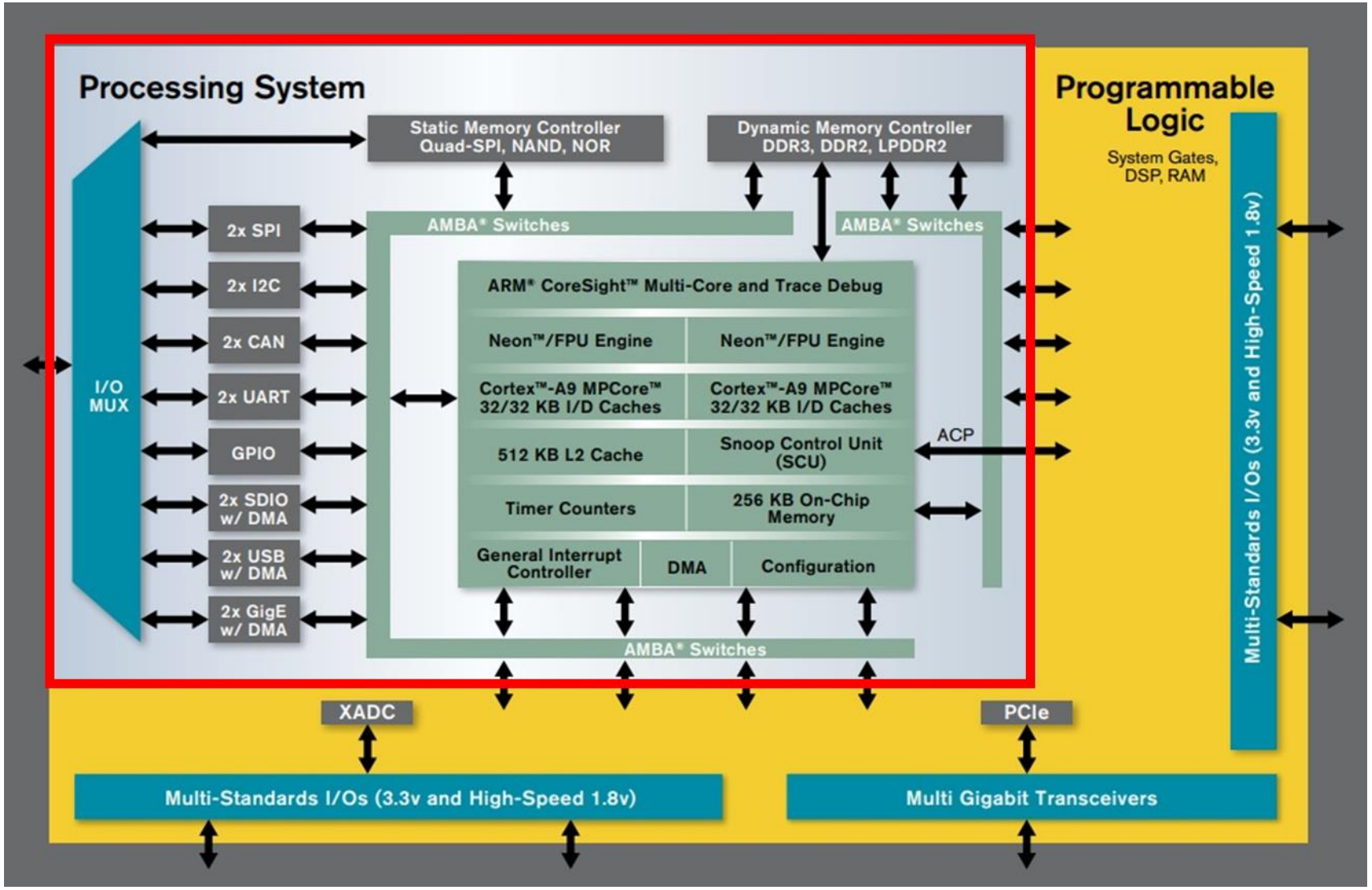
Zynq SoC Block Design



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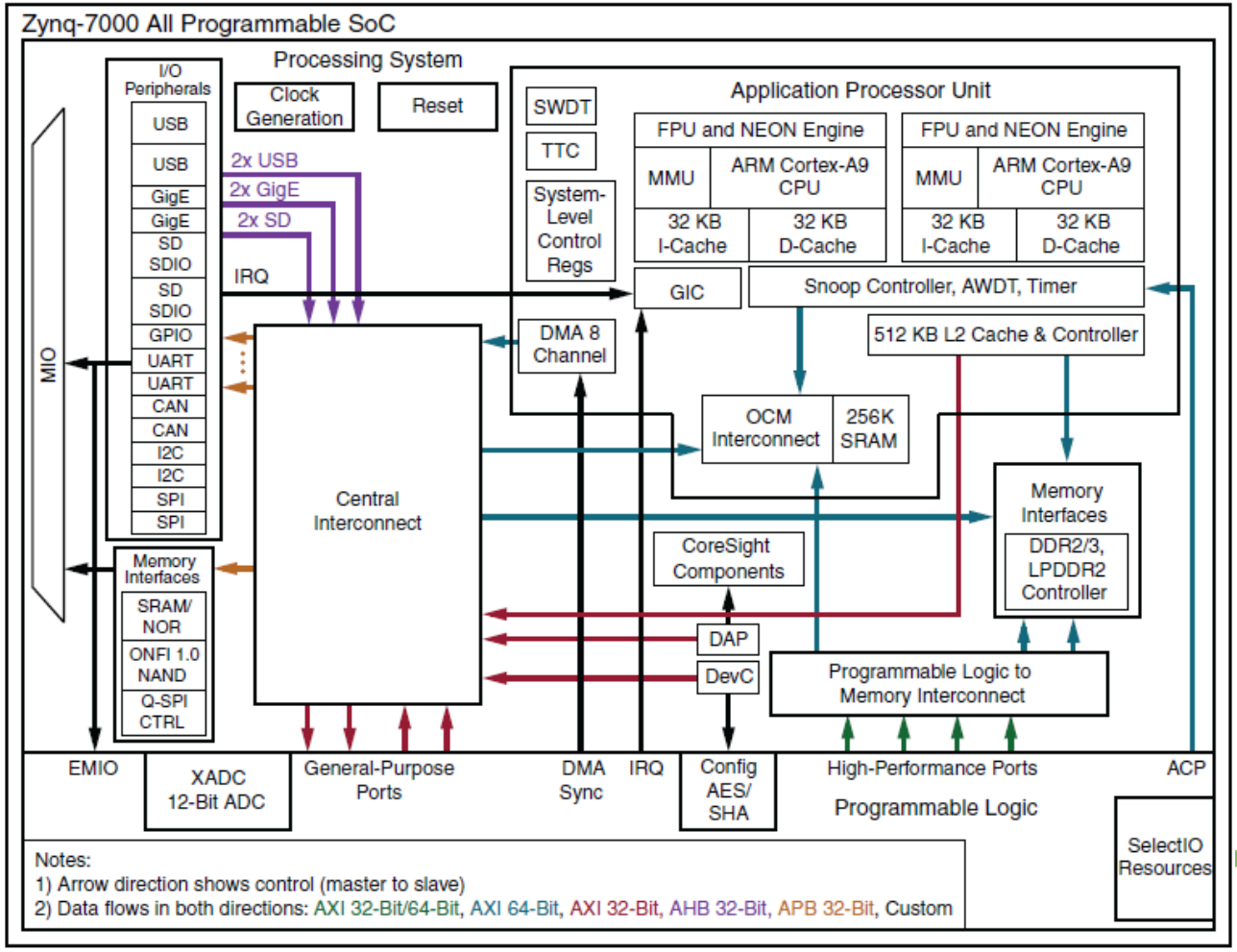
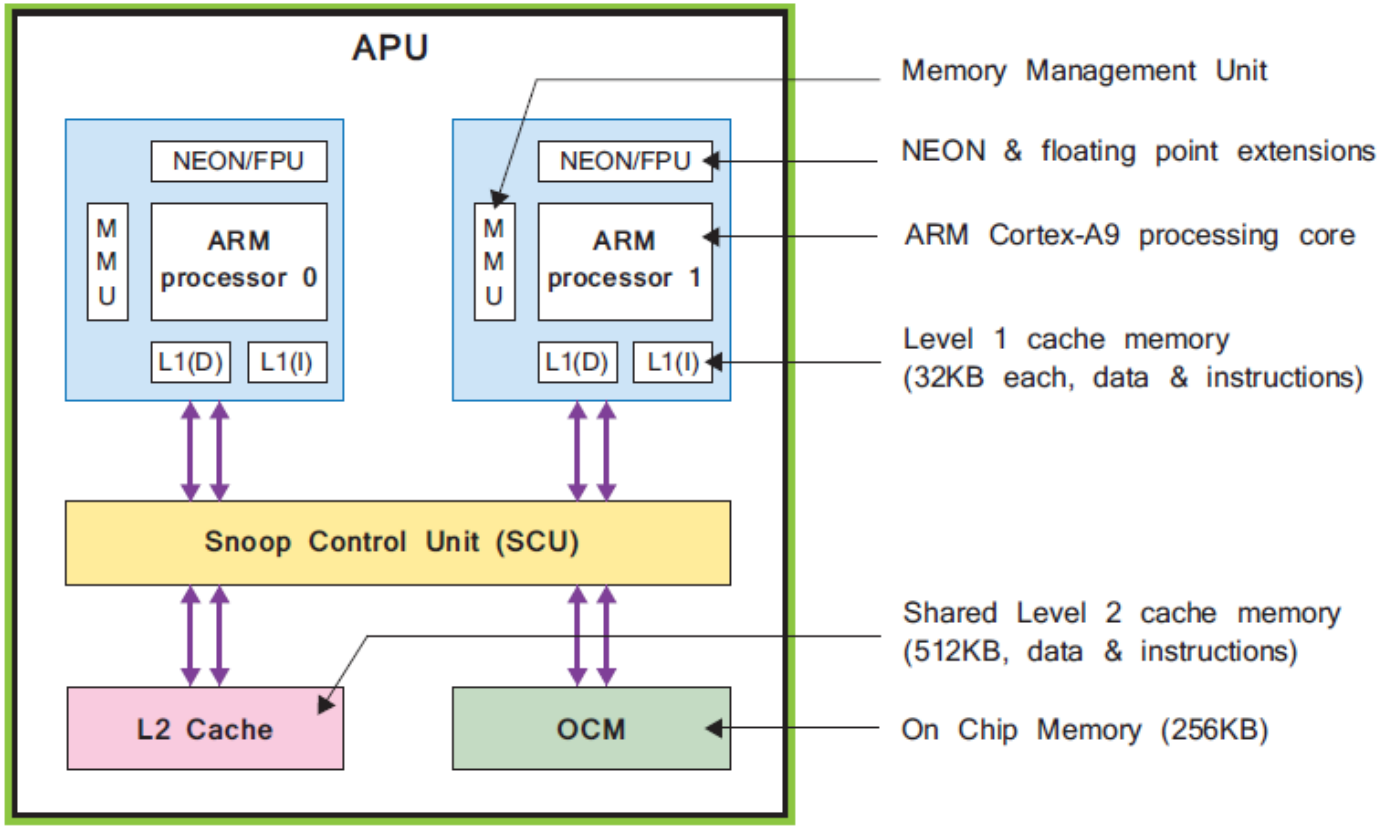
Processing System

- APU
  - ARM Cortex-A9
  - FPU
  - Cache Memory
- I/O Peripherals
- Memory Interface
- Interconnect
- Clock generation



APU

- ARM Cortex-A9 Processor
  - Up to 1GHz
- NEON(MPE) / FPU
- Memory Manage Unit(MMU)
- L1 캐시, L2 캐시
- On Chip Memory
- Snoop Control Unit(SCU)
  - 코어, L1-L2캐시, OCM 브릿지



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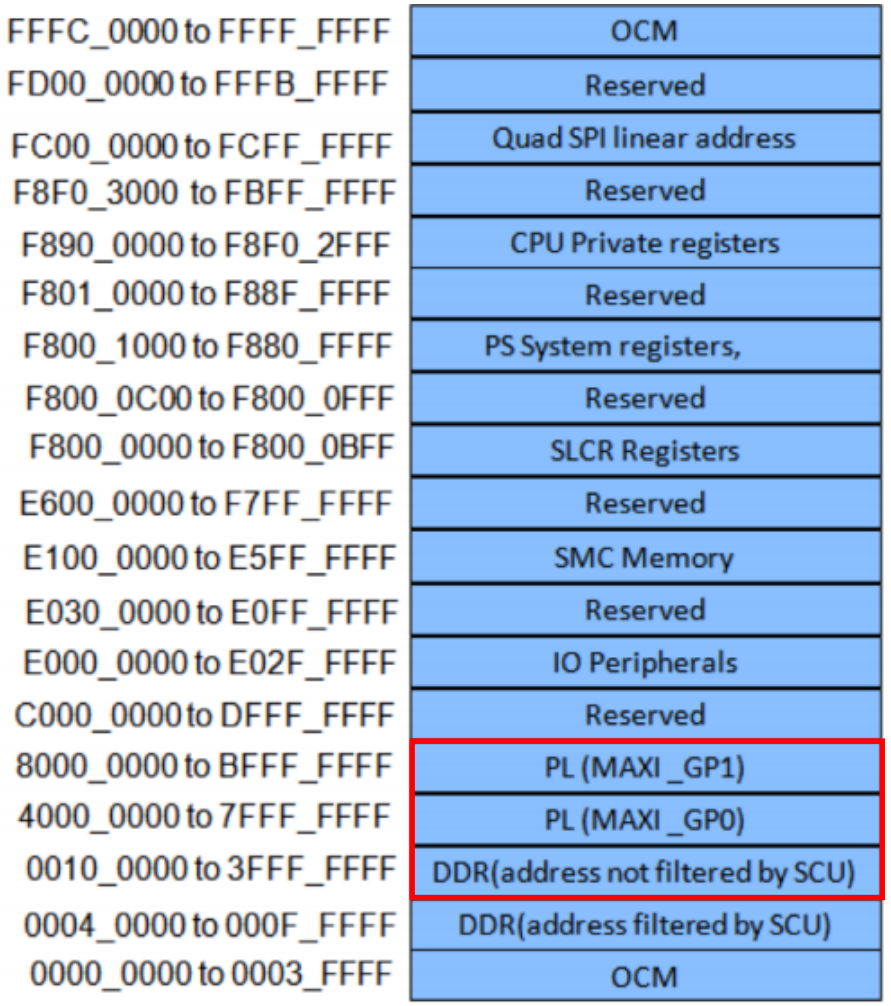
Memory Map

- Cortex-A9 Processor
- 32bit Addressing
  - 4GB Address map
- 모든 PS, PL 주변장치
  - Cortex-A9 프로세서 메모리 매핑

- 0x4000_0000: PL AXI Slave0
- 0x0010_0000: DRAM



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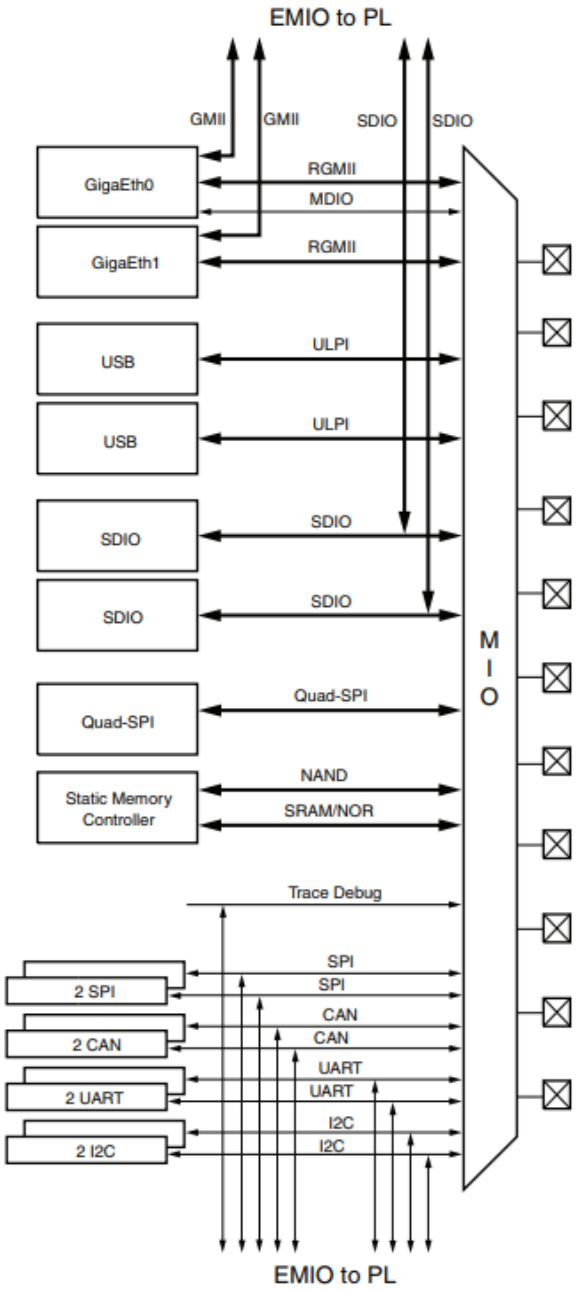
Peripherals

- MIO – PS와 54pin 연결
- EMIO – PL 영역의 외부 핀 연결

- USB 2.0 OTG/Device/Host
- Tri-mode GigE (10/100/1000)
- SD/SDIO Interface
- SPI, CAN, UART, I2C



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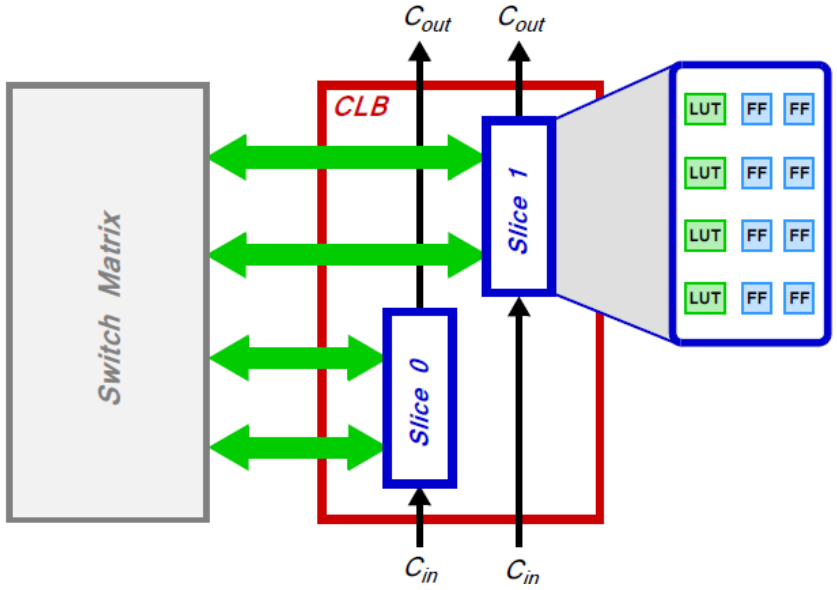
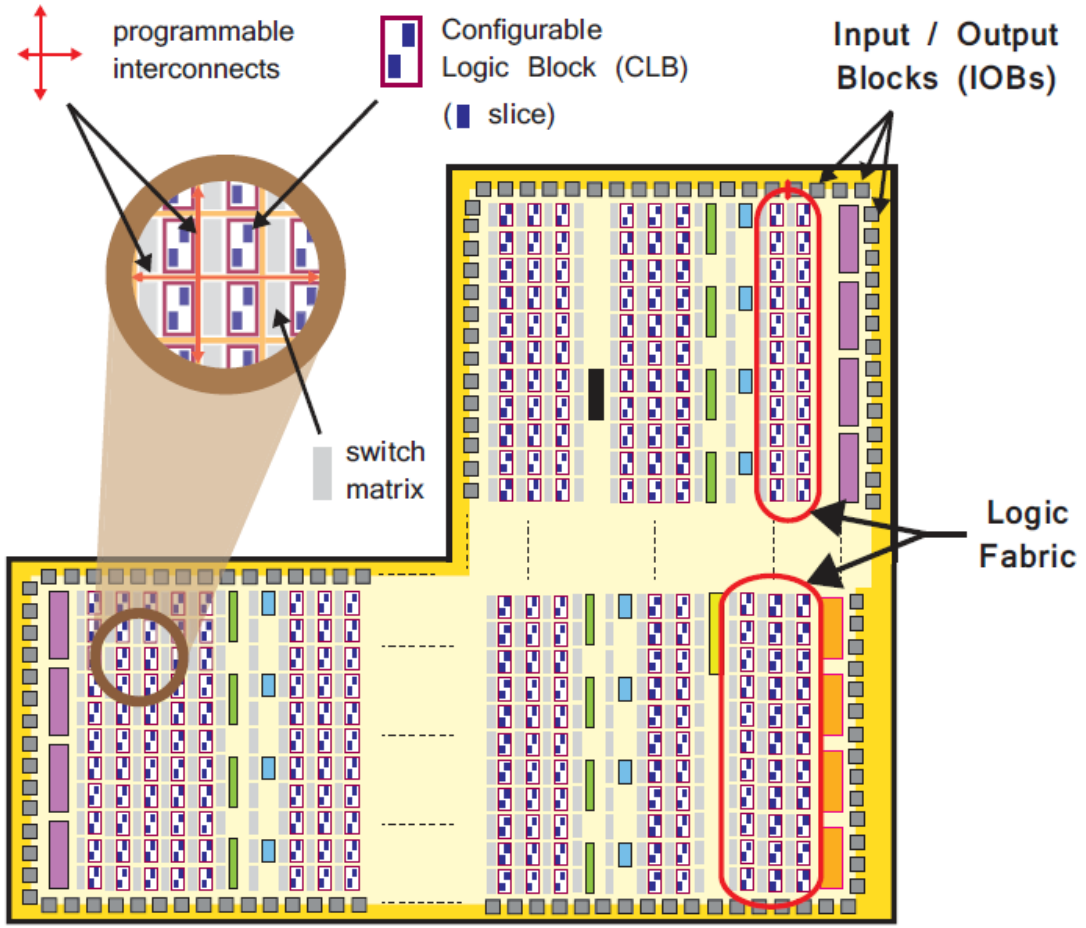
Programmable Logic

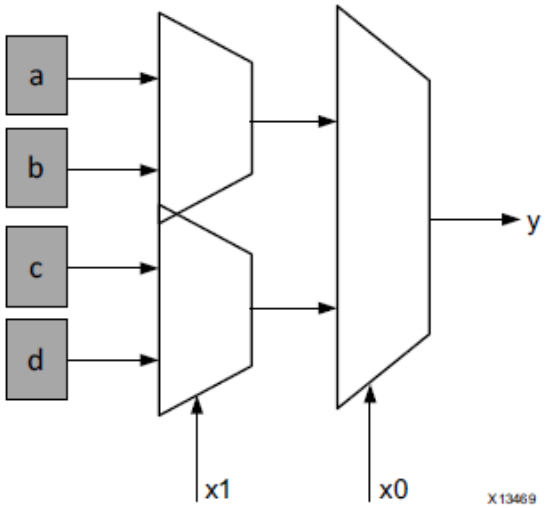
- Configurable Logic Block(CLB)
  - Slice – 4 X LUT, 8 X FF
    - Look-Up Table(LUT)
    - Flip-Flop: 1'b register
- Input/Output Blocks(IOBs)

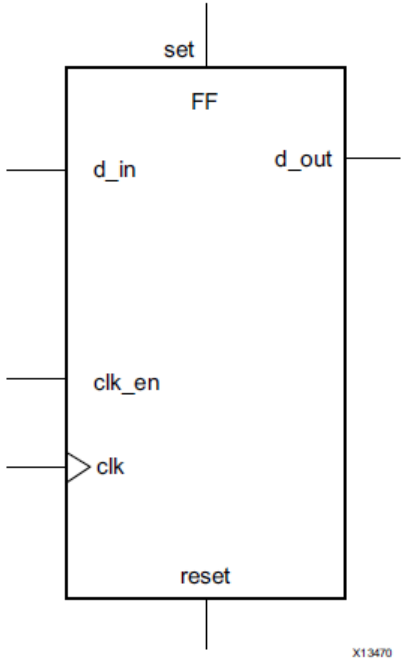




Programmable Logic

- Look-Up Table(LUT)
  - Logic Function
  - ROM(small)
  - RAM(small)
  - Shift Register
- Flip-Flop
  - Sequential circuit(순차 회로)의 1 bit 래치





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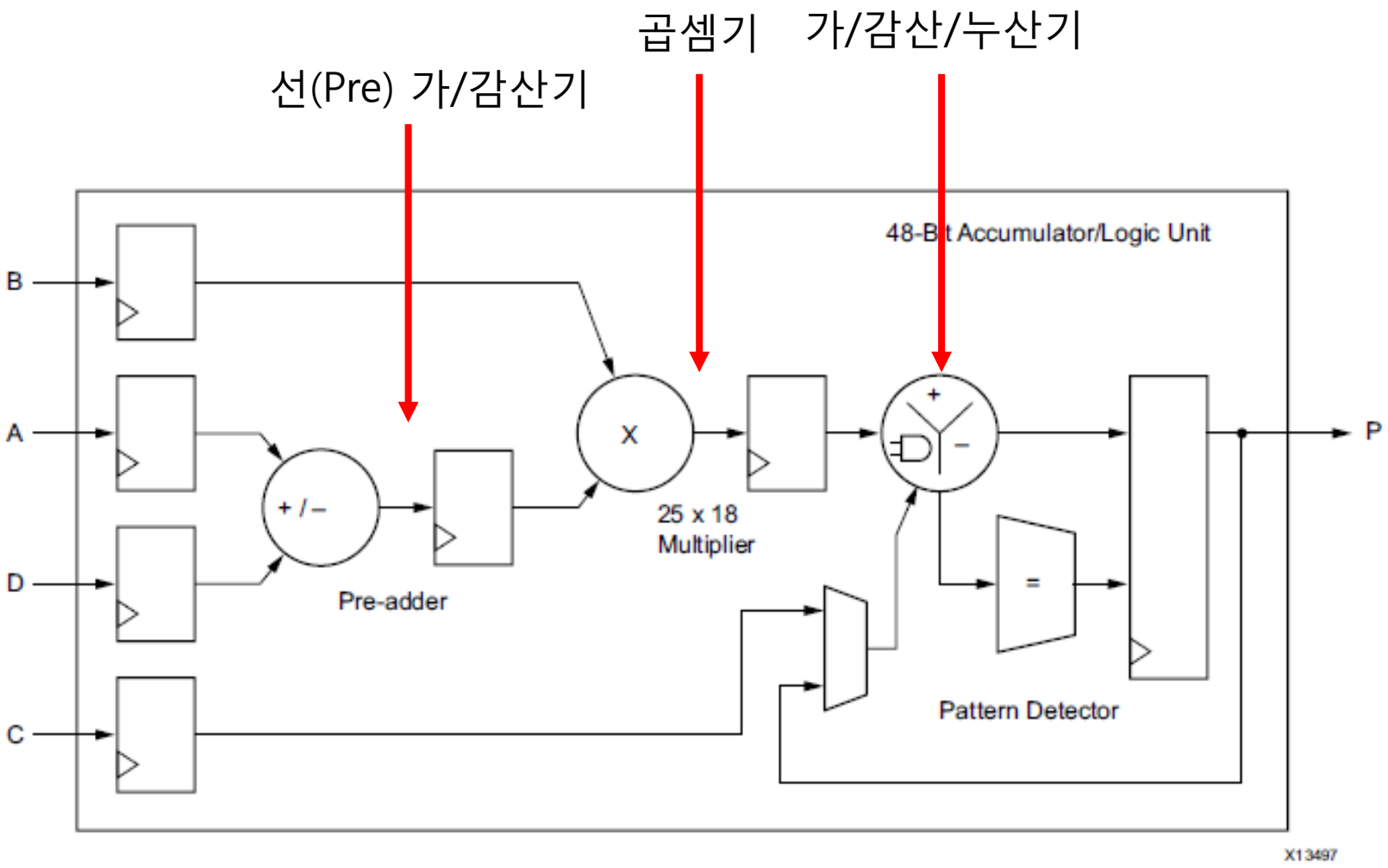
Programmable Logic

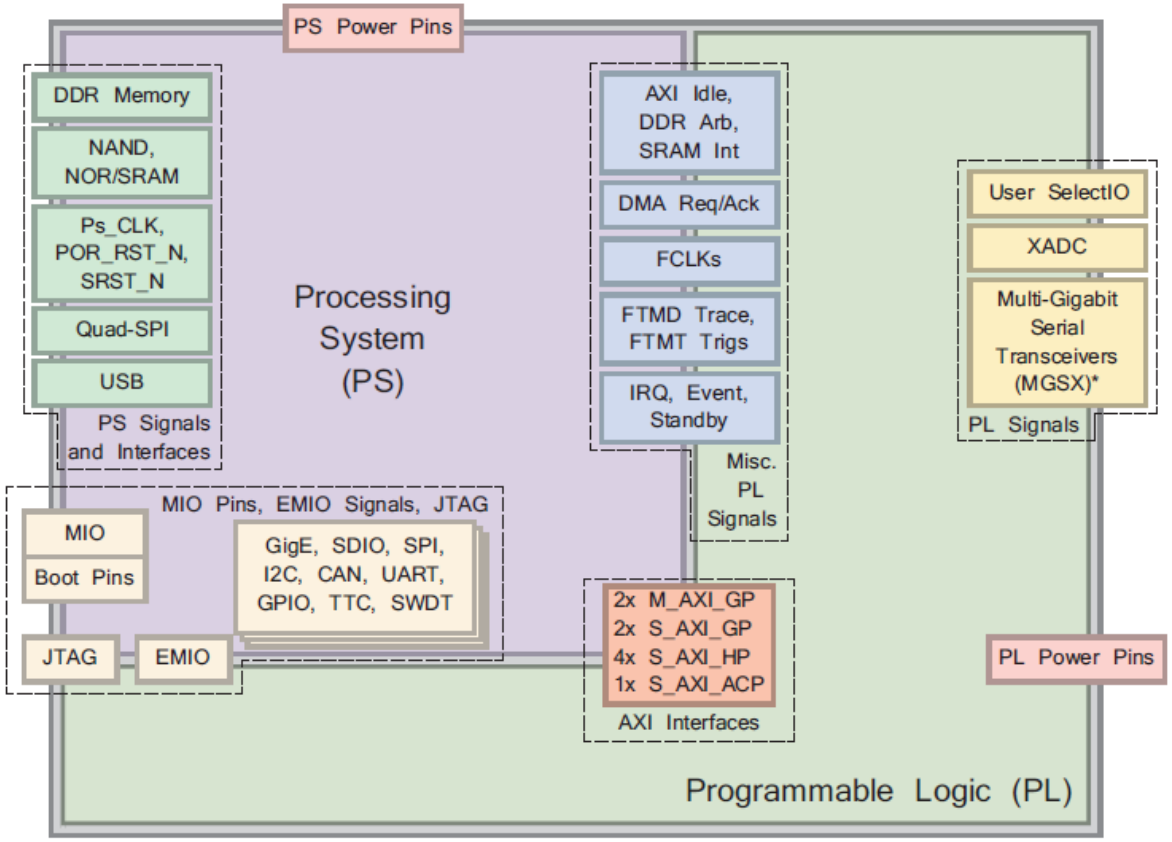
- Block RAM
  - RAM
  - ROM
  - FIFO buffer

- DSP48E1(ALU)
  - 3가지 블록의 조합
  - $p = a \times (b + d) + c$
  - $p \ += a \times (b + d)$



PS-PL Interface

- AXI Interface
  - 32 bit Master-Slave interface
  - High Performance ports
  - 64 bit AXI Slave(ACP) port
- DMA, interrupts, event signals
- EMIO
- Clock(4 PS→PL), Resets(4 PS→PL)
- Configuration



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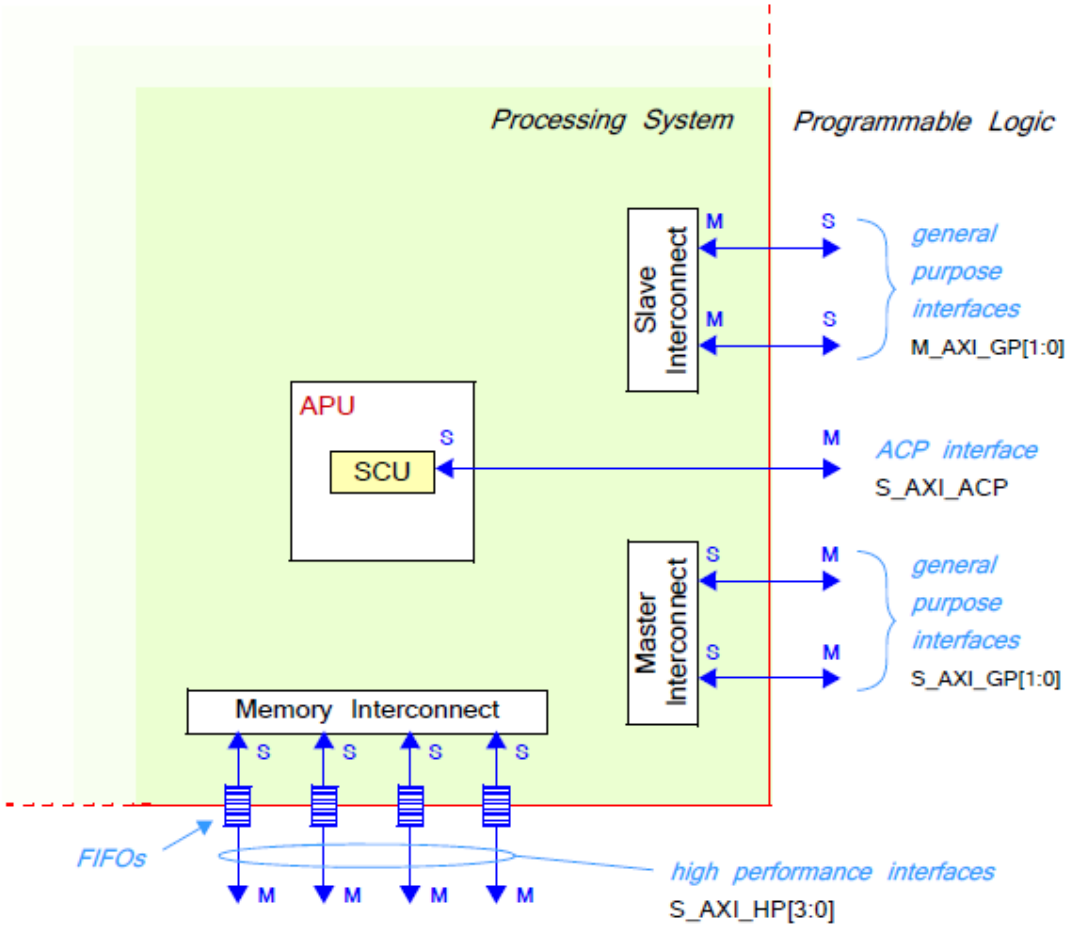
PS-PL AXI Interface

Interface Name	Interface Description	Master	Slave
M_AXI_GP0	General Purpose (AXI_GP)	PS	PL
M_AXI_GP1		PS	PL
S_AXI_GP0	General Purpose (AXI_GP)	PL	PS
S_AXI_GP1		PL	PS
S_AXI_ACP	Accelerator Coherency Port (ACP), cache coherent transaction	PL	PS
S_AXI_HP0	High Performance Ports (AXI_HP) with read/write FIFOs. (Note that AXI_HP interfaces are sometimes referred to as AXI Fifo Interfaces, or AFIs).	PL	PS
S_AXI_HP1		PL	PS
S_AXI_HP2		PL	PS
S_AXI_HP3		PL	PS



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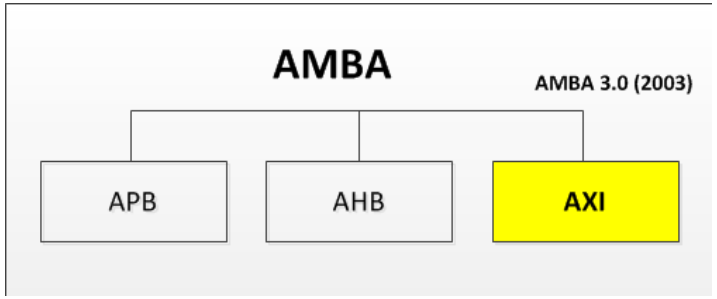
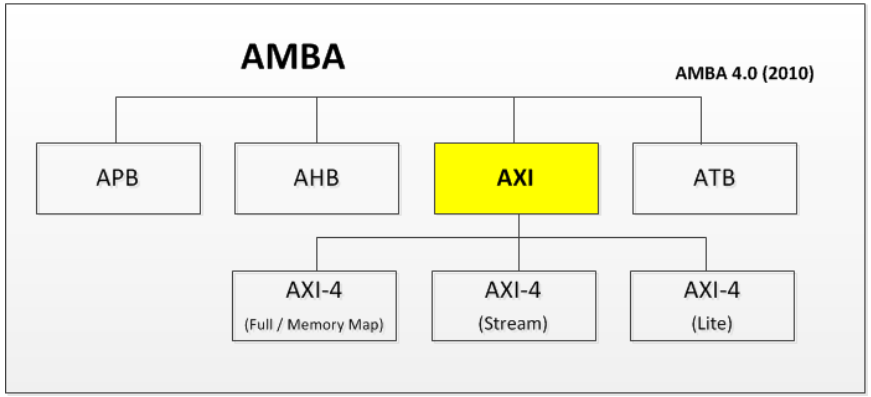
04. AXI AMBA Protocol

- AMBA – ARM에서 발표한 버스 규격
  - Advanced Microcontroller Bus Architecture
- AMBA 2.0
  - AHB (the Advanced High-performance bus)
  - ASB (the Advanced System Bus)
  - APB (the Advanced Peripheral Bus)
- AMBA 3.0
  - AXI (the Advanced extensible Interface)
- AMBA 4.0
  - AXI-4
  - AXI-4 Lite
  - AXI-4 Stream





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AXI Protocol 특징

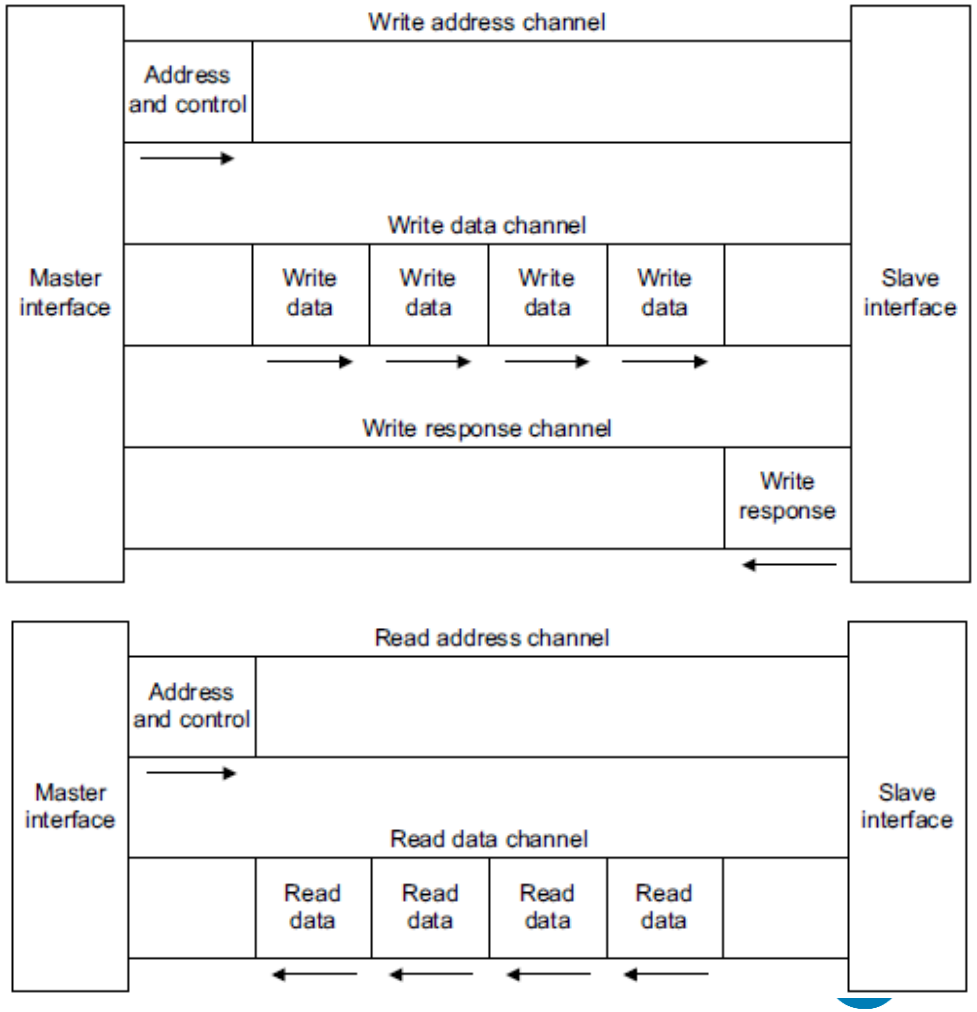
- Address/Control phase와 data phase 구분
- Byte strobe를 이용한 unaligned data 전송
- Start address 만으로 burst-based transactions를 사용
- Read와 Write data channel이 분리되고, Direct Memory Access(DMA) 기능 제공.
- Multiple outstanding address를 발생할 수 있다.
- Out-of-order transaction을 지원

AXI4 Variation

- AXI4 – Address/Data
  - Up to 256 data Transfer / 1 transaction
- AXI4-Lite – Address/Data
  - 1 data transfer / 1 transaction
- AXI4-Stream – Data
  - Unlimited burst

AXI4

- 5개 채널로 구성
  - Write Address Channel
  - Write Data Channel
  - Write Response Channel
  - Read Address Channel
  - Read Data Channel
- Single address, multiple data
  - Burst up to 256 cycle
- Data width
  - 8, 16,…256, 512, 1024



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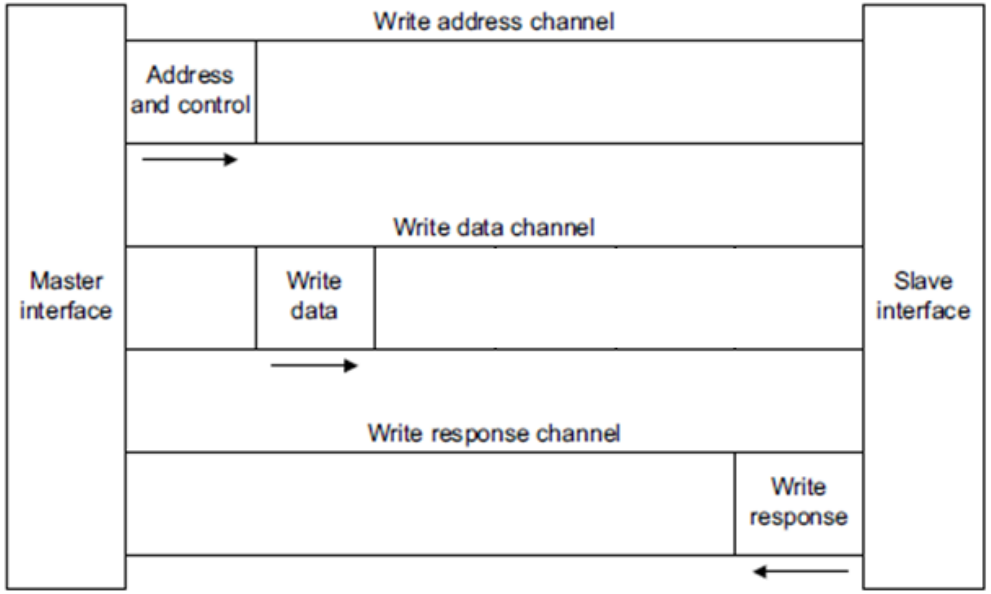
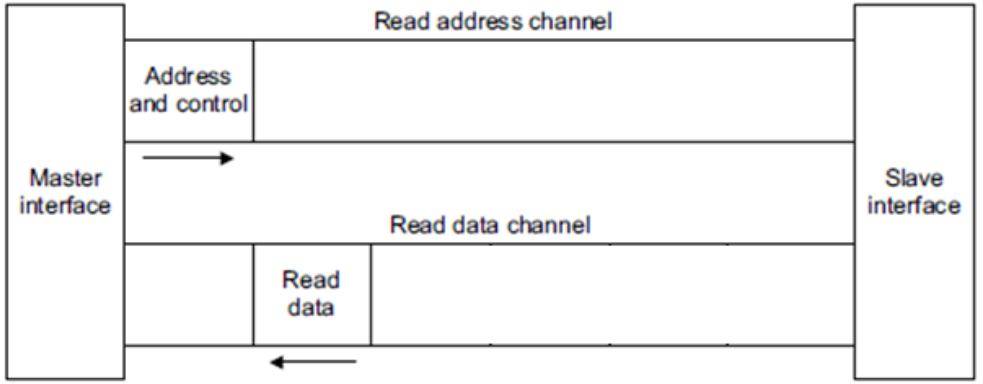
AXI4-Lite

- No data burst
  - Single data transaction
- Data width 32 or 64 bits only
  - Xilinx IP supports 32-bits
- Small footprint





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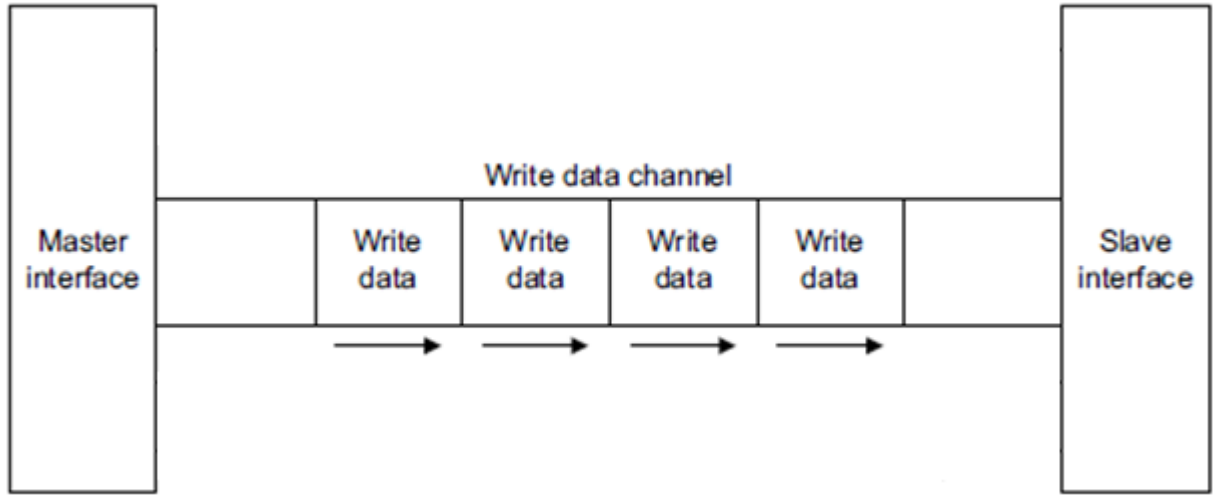
AXI4 Stream

- Write data channel only
- No burst cycle limit



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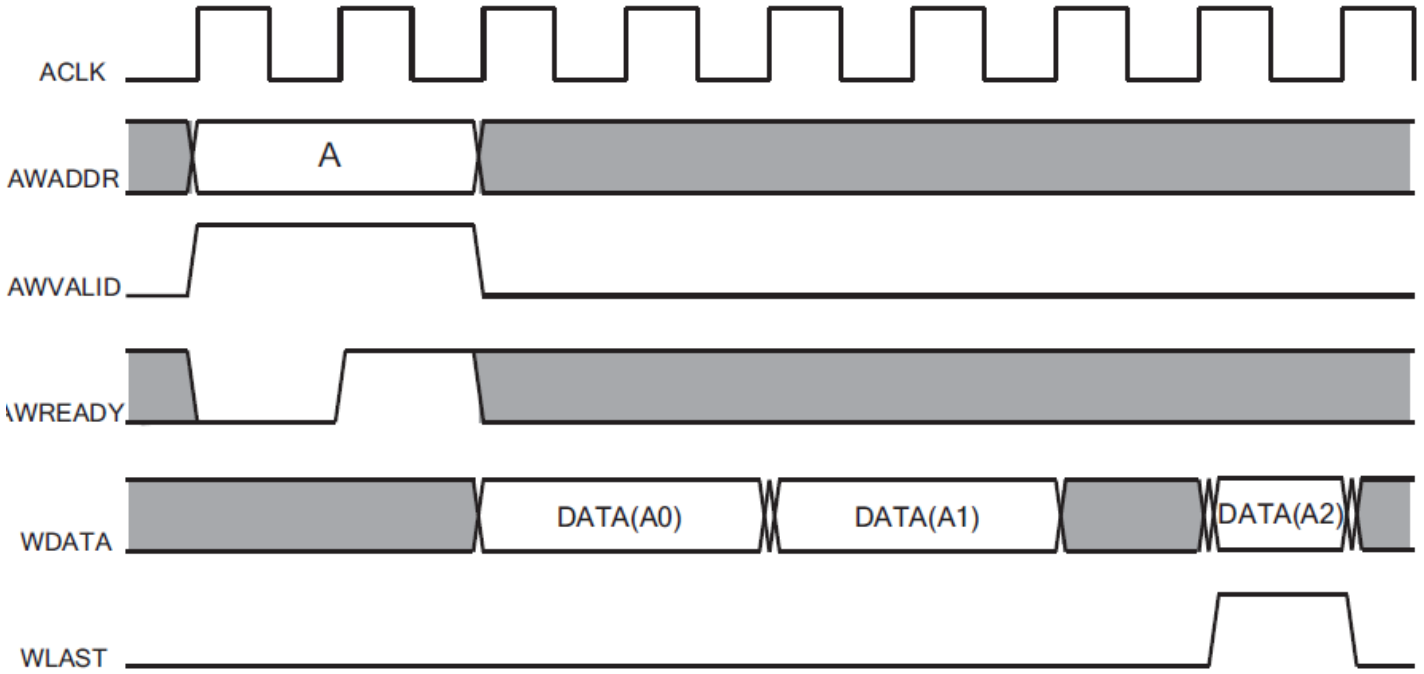
AXI Write Transaction

- Master
  - sets AWADDR
  - sets AWVALID up
- Slave
  - sets AWREADY
- Master
  - clear AWVALID
  - transfer WDATA
  - sets WLAST up when transfer finished



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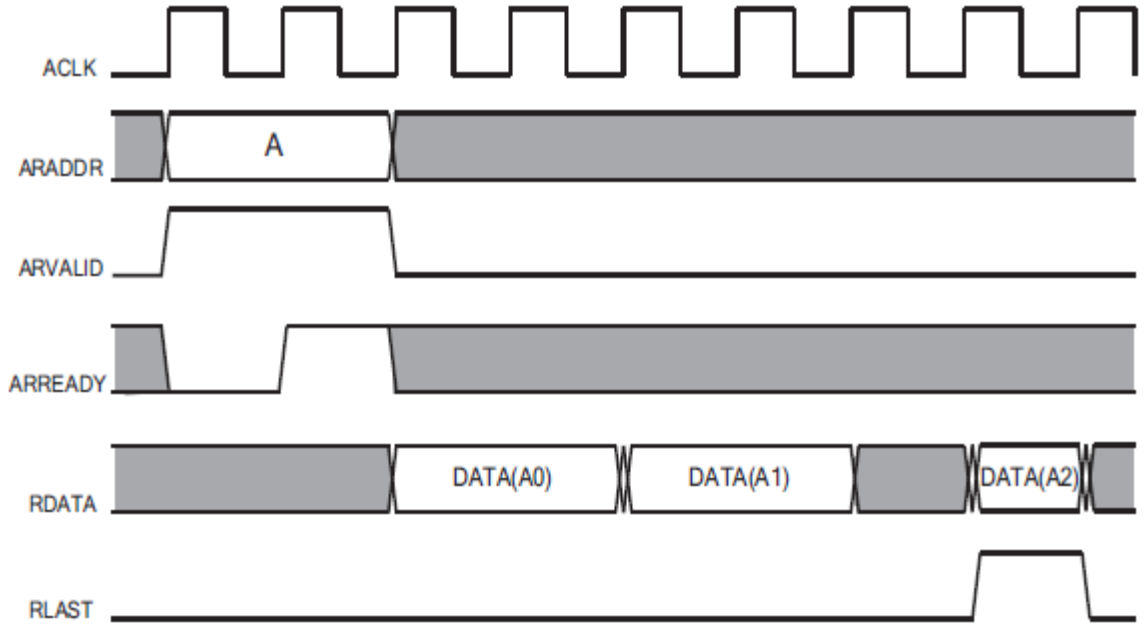
AXI Read Transaction

- Master
  - sets ARADDR
  - sets ARVALID up
- Slave
  - sets ARREADY
  - sets RDATA
  - sets RLAST



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AXI4, AXI4-Lite

AXI4	AXI4-Lite
ACLK	
ARESTN	
AWID	
AWADDR	
AWLEN	
AWSIZE	
AWBURST	
AWLOCK	
AWCACHE	
AWPROT	
AWQOS	
AWSIZE	
AWREGION	
AWLOCK	
AWUSER	
AWVALID	
AWREADY	

Write Address

AXI4	AXI4-Lite
WDATA	WDATA
WSTORB	WSTORB
WLAST	
WUSER	
WVALID	
WREADY	

Write Data

AXI4	AXI4-Lite
BID	
BRESP	BRESP
BUSER	
BVALID	
BREADY	

Write Resp.

AXI4	AXI4-Lite
ARID	
ARADDR	
ARLEN	
ARSIZE	
ARBURST	
ARLOCK	
ARCACHE	ARCACHE
ARPROT	ARPROT
ARQOS	
ARREGION	
ARUSER	
ARVALID	
ARREADY	

Read Address

AXI4	AXI4-Lite
RID	
RDATA	RDATA
RRESP	RRESP
RLAST	
RUSER	
RVALID	
RREADY	

Read Data

ZYNQ를 이용한 SoC 설계 이해

CONTENTS

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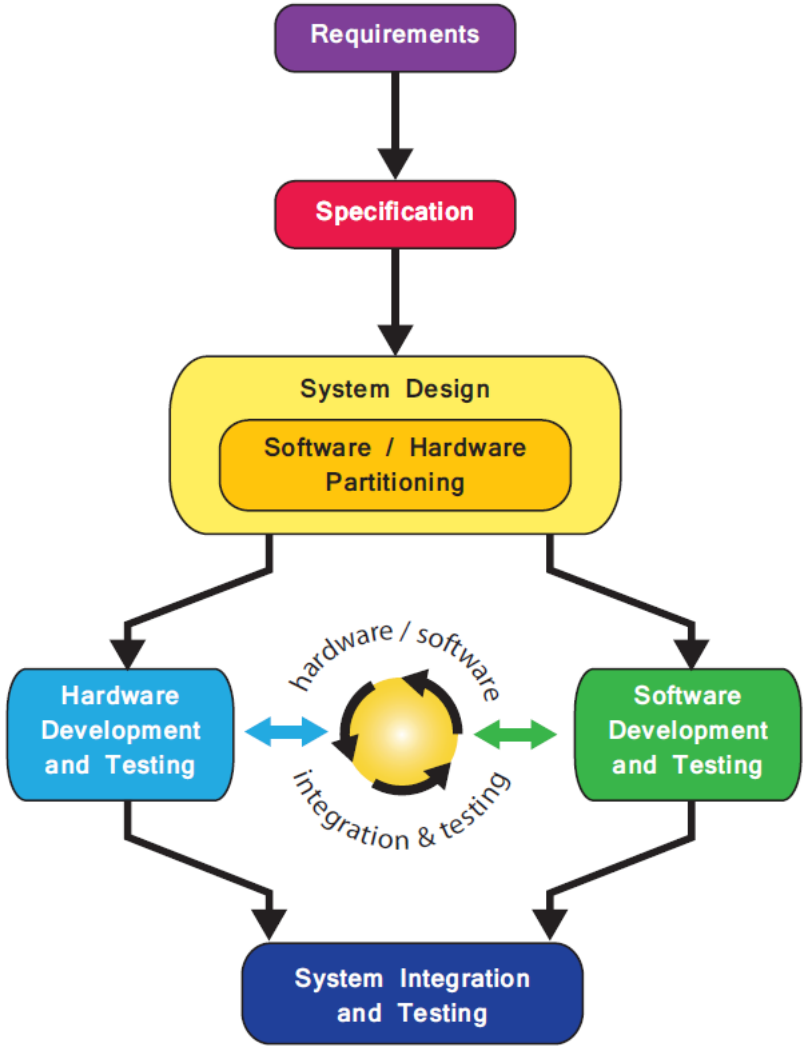
01. Zynq SoC 설계

Xilinx VIVADO

VHDL/Verilog
HLS(SDSoC)

AXI HW IP



Xilinx SDK

Xilinx, ARM
라이브러리

C/C++ SW IP

Bare Metal App
freeRTOS, Linux

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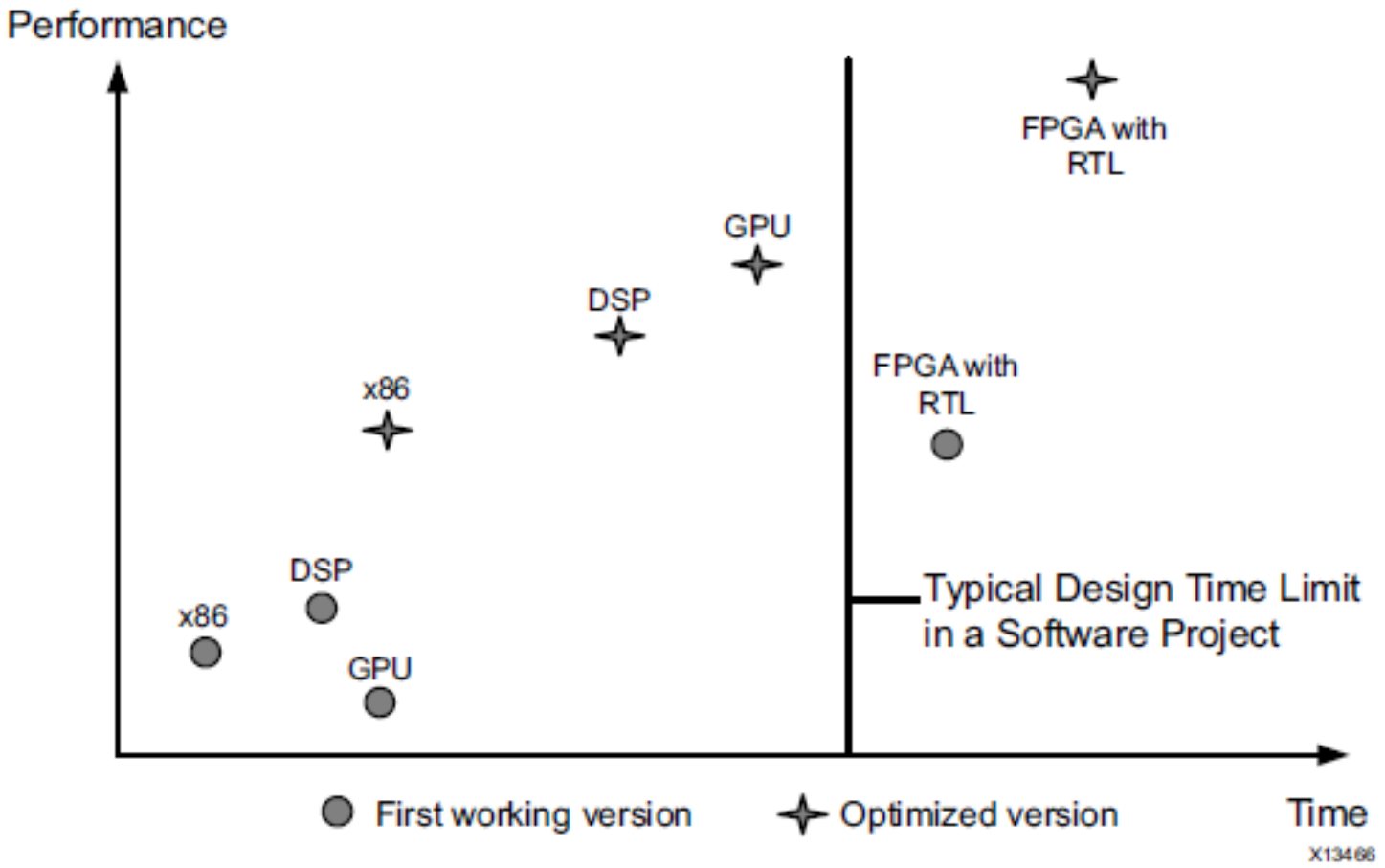
Design Time vs. Performance



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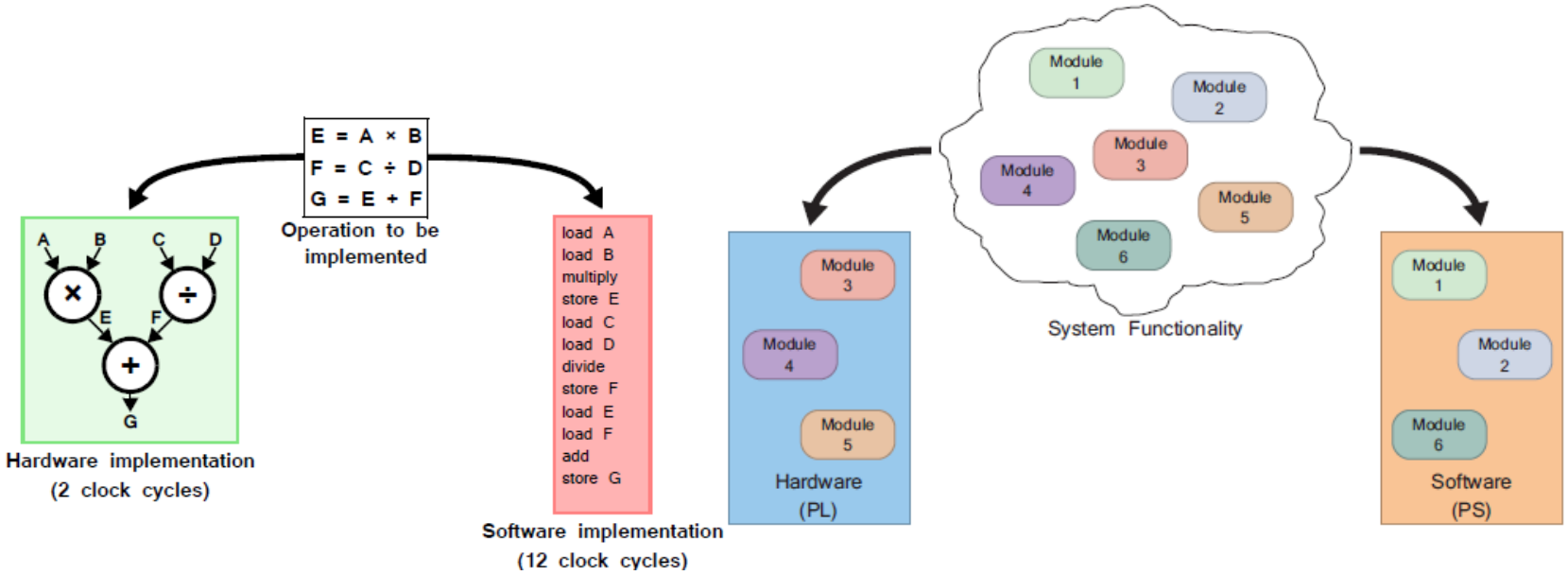
SW/HW Partitioning

- 구현할 기능 SW/HW 구분

- HW
  - 많은 리소스 필요
  - 하드웨어 가속
  - 실시간 처리(영상)
- SW
  - OS
  - User Application
  - GUI



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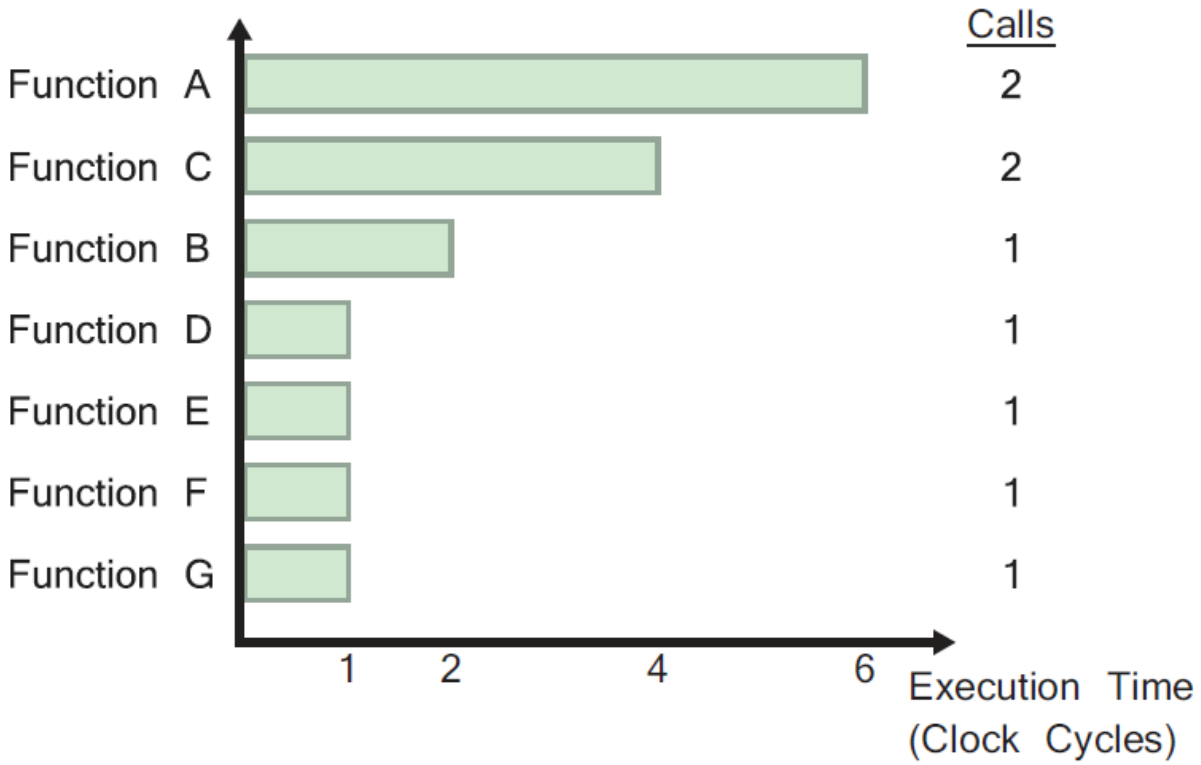
Profiling

- 프로그램 분석
  - Memory
  - Execution time
  - Frequency
  - Instruction usage

- Function A, C
  - Execution time of function call ↑
  - Frequency of function call ↑



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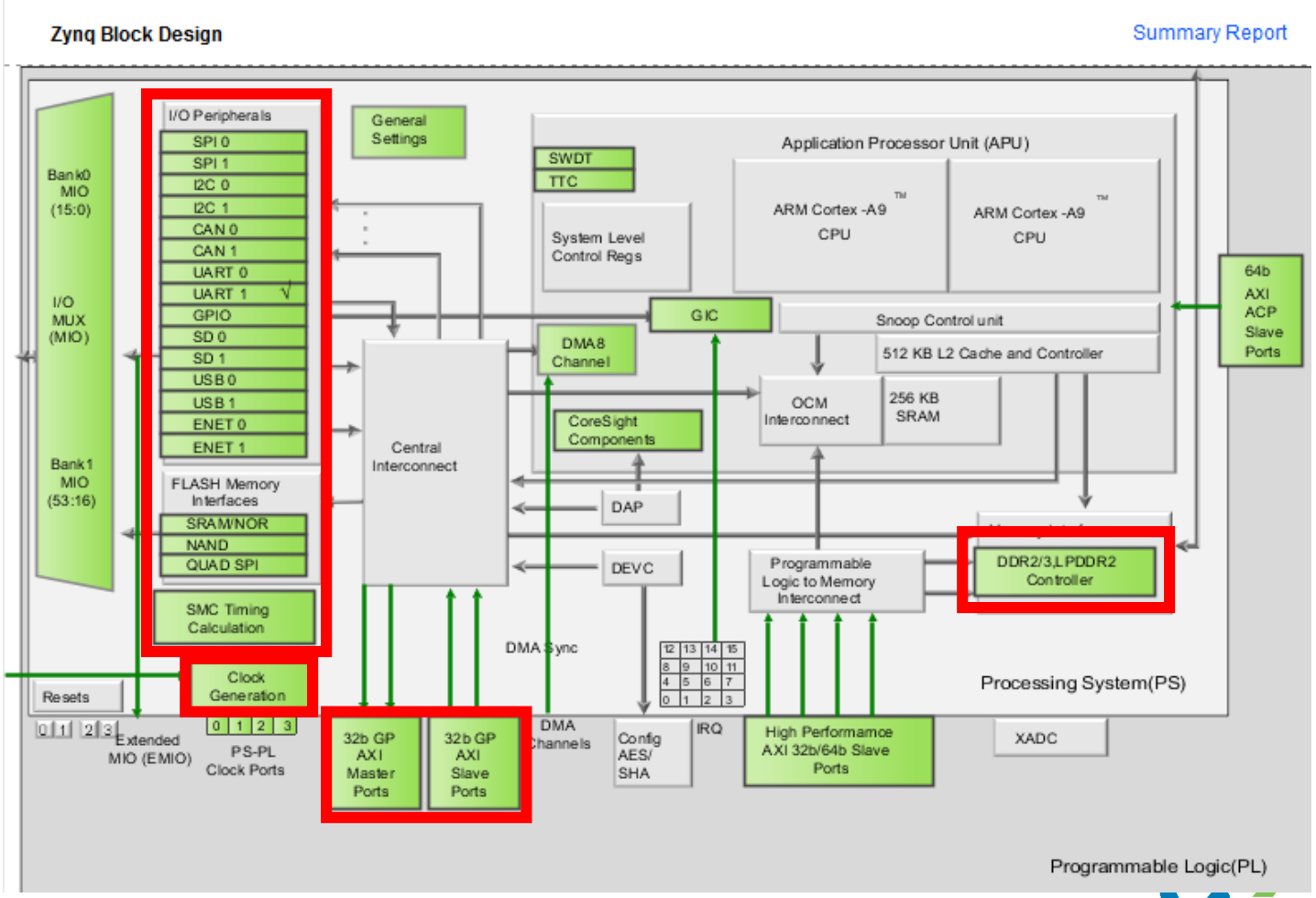
Hardware – PS Configuration

- PS Configuration
  - I/O Peripherals
  - Memory controller
  - Clock generation
  - AXI Interface

- 사용할 IP 선택, 설정



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Hardware – Block Design

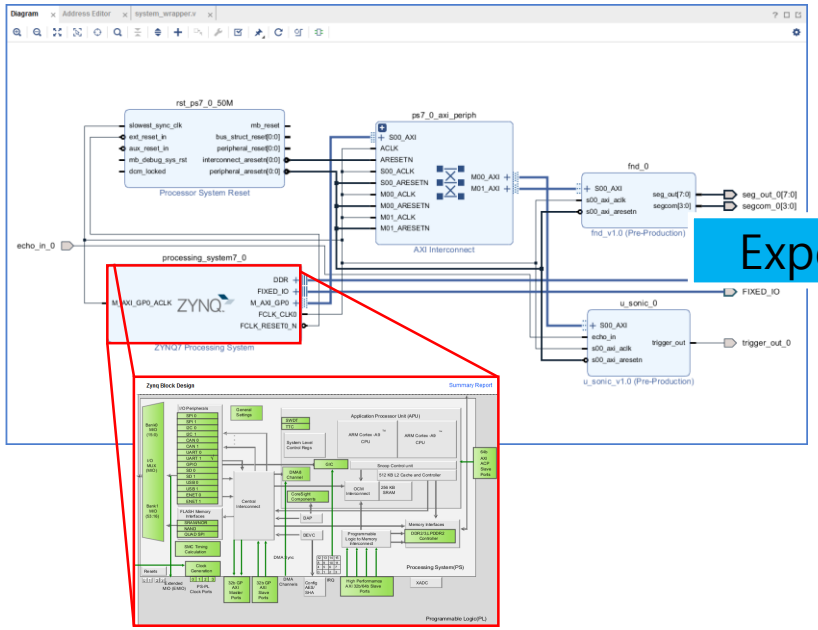
Vivado IDE

Define PS Subsystem

Configure MIO peripherals

Design FPGA Logic

Connect PL <-> PS(Block Design)

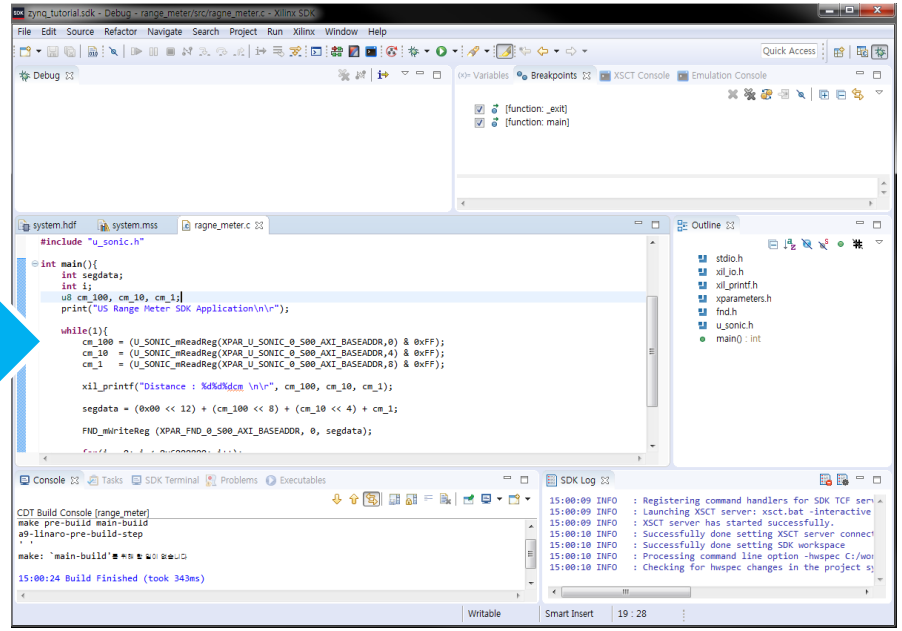


Export HW Design

Software Development Kit(SDK)

애플리케이션 SW 개발/디버그

SDK→ 하드웨어에 맞는 BSP, FSBL 자동 생성



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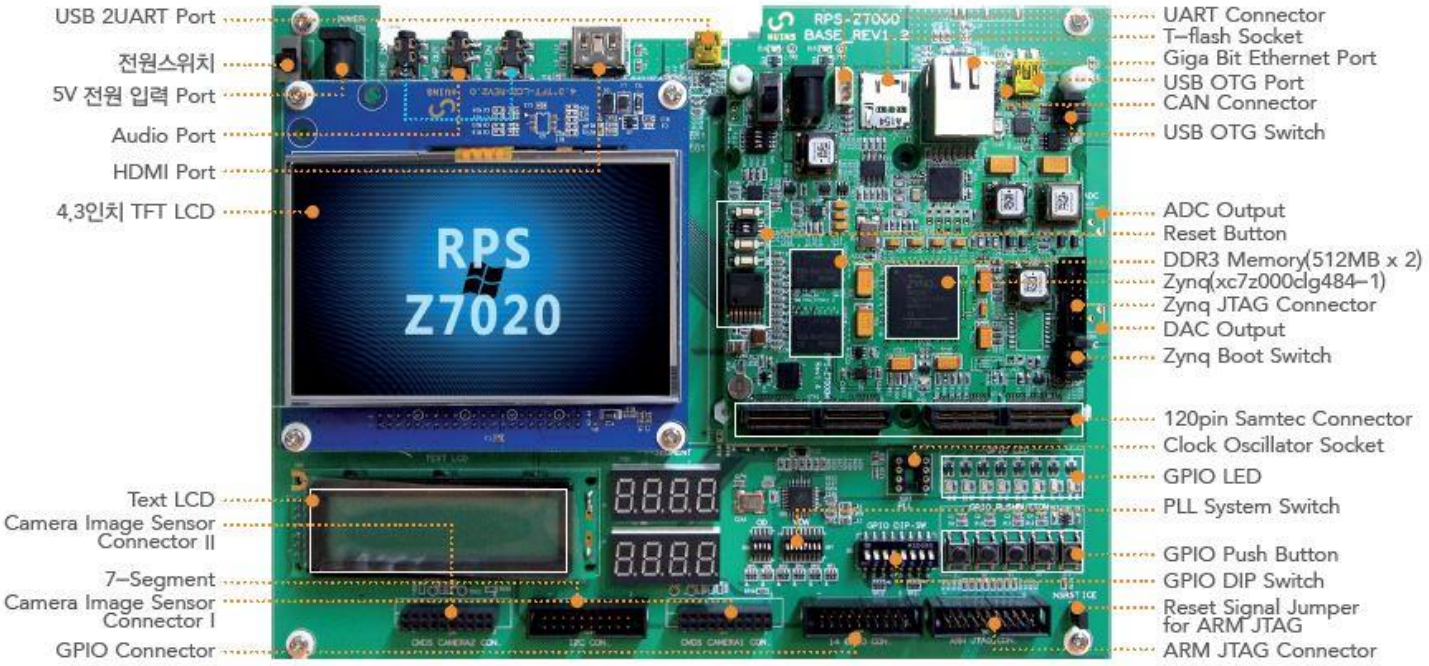
Zynq Development Tool

- Zynq 7020
  - Dual ARM Cortex-A9
  - 85K Artix-7 Logic Cell
- 1GB DDR3 Memory
- Ethernet/USB
- Audio/HDMI
- 주변장치

RPS-Z7020-TK 구성도



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References

- ZYNQ Technical Reference Guide(UG-585)
- THE ZYNQ BOOK(http://www.zynqbook.com)
- Vivado-Intro-FPGA-Design-HLS(UG998)